Abstract

A synchronous dynamic memory has a clock input buffer receiving an external clock and outputting an input external clock, a command input buffer receiving commands, an address input buffer receiving addresses, and a data input buffer receiving data. During normal operation mode, the clock input buffer supplies the clock to the command, address, and data input buffers. During data hold modes, such as power down mode, the clock input buffer supplies the clock to the command input buffer but not to the address and data input buffers.